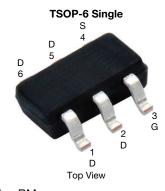


Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) a, e	Q _g (TYP.)			
	0.0210 at V _{GS} = -4.5 V	-8				
-20	0.0240 at V _{GS} = -2.5 V	-8	43.2 nC			
	0.0380 at V _{GS} = -1.8 V	-8				



Marking Code: BM Ordering Information:

Si3429EDV-T1-GE3 (lead (Pb)-free and halogen-free)

FEATURES

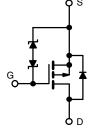
- TrenchFET® power MOSFET
- 100 % R_g tested
- Built-in ESD protection
 - Typical ESD performance 3000 V
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

ROHS COMPLIANT HALOGEN

APPLICATIONS

- Power management for portable and consumer
 - Load switches
 - DC/DC converters



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unless	s otherwise noted	d)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	-20	V	
Gate-Source Voltage		V _{GS}	± 8	v
	T _C = 25 °C		-8 e	
Continuous Drain Current (T. 150 °C)	T _C = 70 °C	l , [-8 e	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	-8 b, c, e	
	T _A = 70 °C		-6.4 ^{b, c}	А
Pulsed Drain Current (t = 300 μs)	I _{DM}	-40		
Continuous Source-Drain Diode Current	T _C = 25 °C		-3.5	
	T _A = 25 °C	l _s	-1.7 ^{b, c}	
	T _C = 25 °C		4.2	
Mariana Darra Dissipation	T _C = 70 °C		2.7	14/
Maximum Power Dissipation	T _A = 25 °C	P _D	2 b, c	W
	T _A = 70 °C		1.3 b, c	
Operating Junction and Storage Temperature R	T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum Junction-to-Ambient b, d	t ≤ 5 s	R _{thJA}	45	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	25	30	- C/W	

Notes

- a. $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. Maximum under steady state conditions is 110 °C/W.
- e. Package limited.



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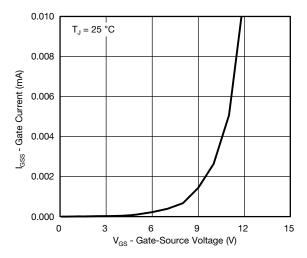
SPECIFICATIONS (T _J = 25 °C, t		,					
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				1		I	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = -250 μA	-	-12	-	mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	2 ,	-	2.4	-		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.4	-	-1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 10	- μΑ	
	400	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	-	-	± 1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μ	
Zoro dato Voltago Brain Gamont	יטסט	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$	-	-	-10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-15	-	-	Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -4 \text{ A}$	-	0.0175	0.0210	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -4 \text{ A}$	-	0.0200	0.0240		
		$V_{GS} = -1.8 \text{ V}, I_D = -2 \text{ A}$	-	0.0250	0.0380		
Dynamic ^b							
Input Capacitance	C _{iss}		-	4083	-	pF	
Output Capacitance	Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	395	-		
Reverse Transfer Capacitance	C _{rss}		-	365	-		
	Q _g	V _{DS} = -10 V, V _{GS} = -8 V, I _D = -8 A	-	78.2	118	;	
Total Gate Charge			-	43.2	65	nC	
Gate-Source Charge		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -8 \text{ A}$	-	6.3	-		
Gate-Drain Charge	Q _{gd}		-	4.3	-		
Gate Resistance	Rg	f = 1 MHz	1.8	9.4	18.8	Ω	
Turn-On Delay Time	t _{d(on)}		-	35	53		
Rise Time	t _r	$V_{DD} = -10 \text{ V, R}_{1} = 1.56 \Omega$	-	30	45		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -6.4 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	174	261		
Fall Time	t _f		-	58	87		
Turn-On Delay Time	t _{d(on)}		-	10	20	ns	
Rise Time	t _r	$V_{DD} = -10 \text{ V, R}_{1} = 1.56 \Omega$	-	17	26		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -6.4 \text{ A}, V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$	-	210	315		
Fall Time	t _f		-	64	96		
Drain-Source Body Diode Characteristi	cs			l		L	
Continuous Source-Drain Diode Current	Is	T _C = 25 °C		-	-3.5		
Pulse Diode Forward Current	I _{SM}		-	-	-40	Α	
Body Diode Voltage	V _{SD}	I _S = -6.4 A, V _{GS} = 0 V	-	-0.8	-1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	28	42	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	16	24	nC	
Reverse Recovery Fall Time	ta	$I_F = -6.4 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 °C$	-	13	-	 	
•	erse Recovery Rise Time t _b			1	ı	ns	

Notes

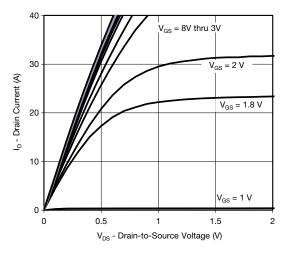
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

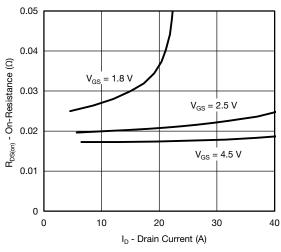




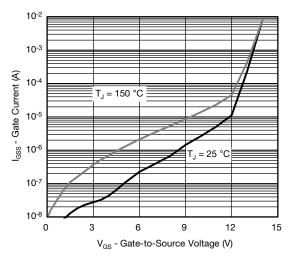
Gate Current vs. Gate-Source Voltage



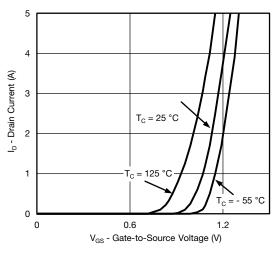
Output Characteristics



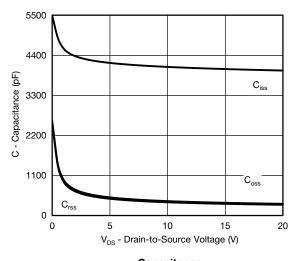
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage

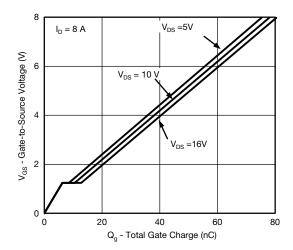


Transfer Characteristics

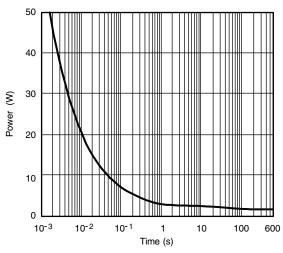


Capacitance

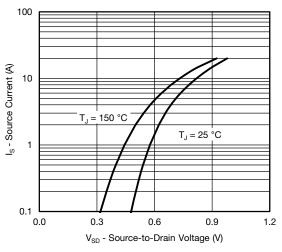




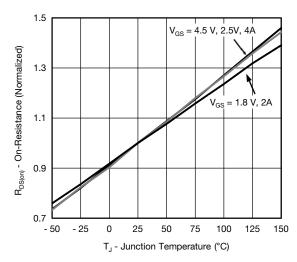
Gate Charge



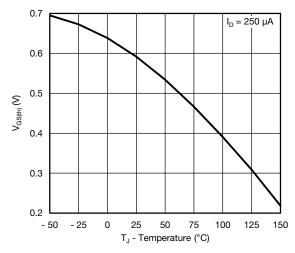
Single Pulse Power, Junction-to-Ambient



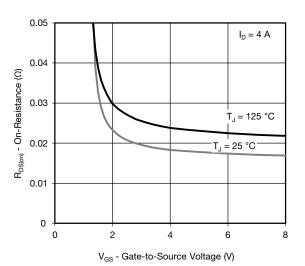
Source-Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature

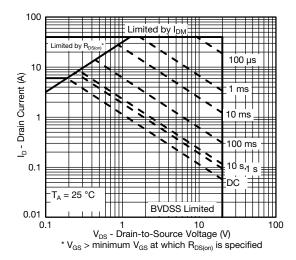


Threshold Voltage

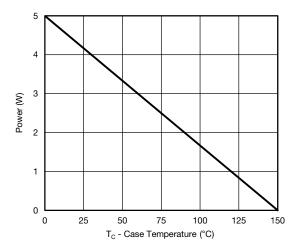


On-Resistance vs. Gate-to-Source Voltage

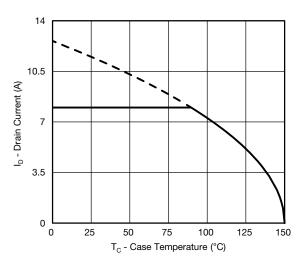




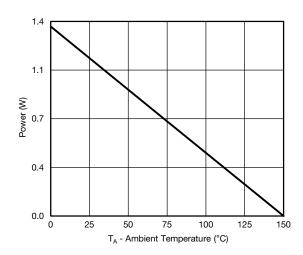
Safe Operating Area, Junction-to-Ambient



Power Junction-to-Foot



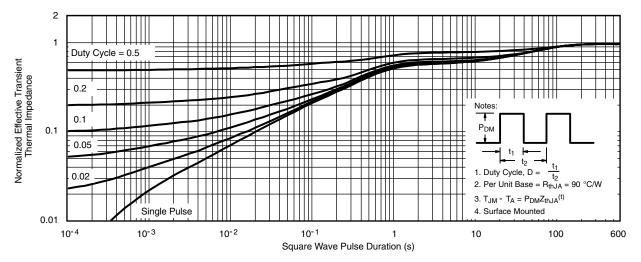
Current Derating*



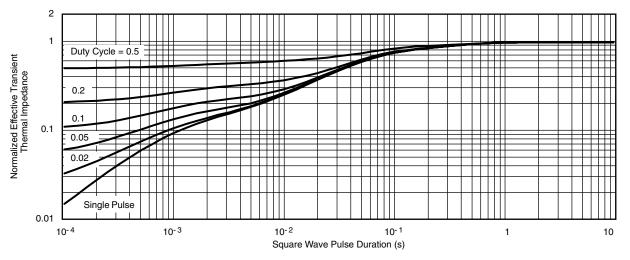
Power Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150 \,^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

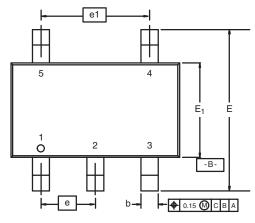
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg262946.

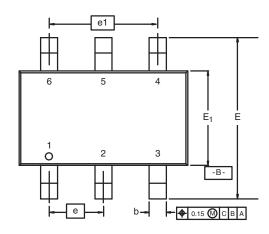




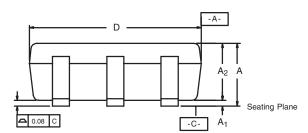
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C

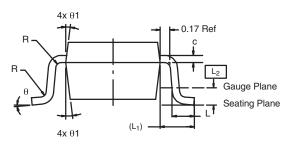




5-LEAD TSOP





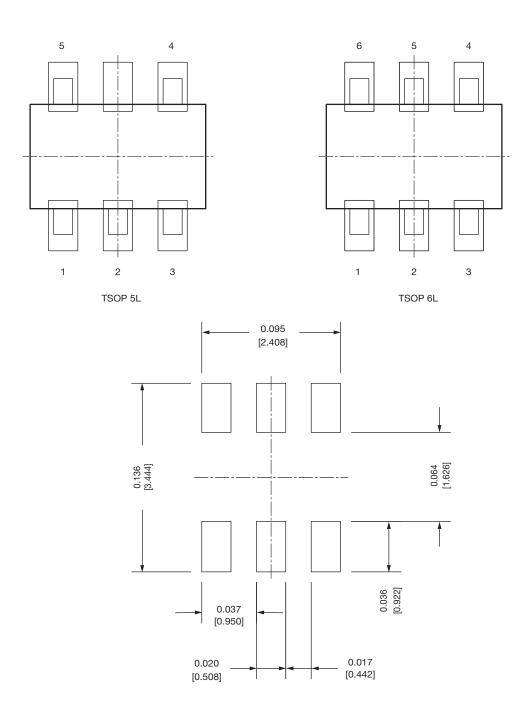


	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е	0.95 BSC			0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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